In the Claims:

The listing of Claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claims 1-133 (Canceled).

134. (Currently Amended) A method of fabricating a metal-semiconductor field-effect transistor comprising:

forming a p-type epitaxial layer of selectively doped p-type conductivity silicon carbide on a single crystal silicon carbide substrate, wherein the p-type conductivity silicon carbide has a carrier concentration of from about 1×10^{16} to about 1×10^{17} cm^{-3}; then

forming an n-type epitaxial layer of n-type conductivity silicon carbide on the p-type epitaxial layer, wherein the n-type epitaxial layer forms a mesa having sidewalls extending into the n-type layer which define the periphery of the transistor;

forming ohmic contacts on the n-type epitaxial layer that respectively define a source and a drain; and

forming a Schottky metal contact on the n-type epitaxial layer that is between the ohmic contacts and thereby between the source and the drain; and

forming an ONO passivation layer on the sidewalls of the mesa and exposed portions of the n-type epitaxial layer.

135. (Original) A method according to Claim 134 further comprising the step of etching the n-type epitaxial layer and the p-type epitaxial layer to form a mesa.

136. (Currently Amended) A method according to Claim 134, wherein the steps of forming ohmic contacts and forming a Schottky gate contact are preceded by the steps of:

etching the n-type epitaxial layer and the p-type epitaxial layer to form a mesa; and

forming an ONO passivation layer on [[the]] exposed surfaces of the mesa.

137. (Original) A method according to Claim 136, wherein the step of forming an ONO passivation layer comprises the steps of:

high temperature annealing exposed portions of the substrate, p-type epitaxial layer and n-type epitaxial layer in an H_2 ambient; then

forming an SiO_2 layer on the exposed portions of the substrate, p-type epitaxial layer and n-type epitaxial layer; then

argon annealing the SiO_2 layer; then

oxidizing the SiO_2 layer; then

depositing a layer of Si_3N_4 on the oxidized SiO_2 layer; then

oxidizing the layer of Si_3N_4.

138. (Original) A method according to Claim 137, wherein the high temperature anneal is carried out at a temperature of greater than about 900 °C for a time of from about 15 minutes to about 2 hours.

139. (Original) A method according to Claim 137, wherein the argon anneal is carried out at a temperature of about 1200 °C for a time of about 1 hour.

140. (Original) A method according to Claim 137, wherein the step of forming an SiO_2 layer comprises the step of forming an SiO_2 layer to a thickness of from about 50 to about 500 Å.

141. (Original) A method according to Claim 137, wherein the step of forming an SiO_2 layer comprises forming an SiO_2 layer through a dry oxide process at a temperature of about 1200 °C.

142. (Original) A method according to Claim 137, wherein the step of oxidizing the SiO_2 layer comprises the step of oxidizing the SiO_2 layer in a wet environment at a temperature of about 950 °C for a time of about 180 minutes.

Claim 143 (Canceled).

Claim 143 (Canceled).

144. (Original) A method according to Claim 137, wherein the step of oxidizing the layer of Si_3N_4 comprises the step of oxidizing the Si_3N_4 layer in a wet environment at a temperature of about 950 °C for a time of about 180 minutes.

145. (Original) A method according to Claim 137, wherein the step of oxidizing the layer of Si_3N_4 comprises the step of oxidizing the Si_3N_4 layer to provide an oxide layer having a thickness of from about 20 to about 200 Å.

146. (Original) A method according to Claim 137, wherein the step of depositing a layer of Si_3N_4 on the oxidized SiO_2 layer is preceded by the step of annealing the oxidized SiO_2 layer in a NO environment.

147. (Original) A method according to Claim 134, further comprising the step of forming a gate recess in the n-type epitaxial layer and wherein the step of forming a Schottky gate contact comprises the step of forming a Schottky gate contact in the gate recess.

148. (Original) A method according to Claim 147, further comprising the step of:

etching through the ONO passivation layer and into the n-type epitaxial layer so as to provide a gate recess in the n-type epitaxial layer; and

wherein the step of forming a Schottky gate contact comprises the step of forming a Schottky gate contact in the gate recess utilizing the ONO passivation layer as a mask.

149. (Original) A method according to Claim 148, wherein the step of etching through the ONO passivation layer is followed by the step of patterning the ONO passivation layer so as to provide a ledge in sidewalls of the opening of the ONO passivation layer for the gate recess; and

wherein the step of forming a Schottky gate contact in the gate recess comprises the step of forming a mushroom gate structure in the gate recess and on the sidewalls and ledge of the ONO passivation layer.

150. (Original) A method according to Claim 148, wherein the step of etching through the ONO passivation layer is carried out by at least one of Electron Cyclotron Resonance and Inductively Coupled Plasma etching.

151. (Original) A method according to Claim 147, wherein the step of forming a gate recess is preceded by the steps of:

forming a cap layer of silicon carbide on the n-type epitaxial layer;

etching through the cap layer to provide a first recess;

wherein the step of forming an ONO passivation layer comprises forming an ONO passivation layer on the cap layer;

etching through the ONO passivation layer and into the n-type epitaxial layer so as to provide a second recess in the n-type epitaxial layer, wherein the second recess is within the first recess; and

wherein the step of forming a Schottky gate contact comprises the step of forming a Schottky gate contact in the second recess utilizing the ONO passivation layer as a mask.

152. (Original) A method according to Claim 134, further comprising the step of implanting n^+ well regions in the n-type epitaxial layer so as to provide source and drain regions and wherein the step of forming ohmic contacts comprises the step of forming ohmic contacts on the n^+ well regions.

153. (Original) A method according to Claim 134, further comprising the steps of:

thinning the substrate; and then

forming a metallization layer on the substrate opposite the p-type epitaxial layer.

154. (Original) A method according to Claim 153, wherein the step of forming a metallization layer comprises the steps of:

forming a titanium layer on the substrate opposite the p-type epitaxial layer; then

forming a layer of platinum on the titanium layer; and then

forming a layer of gold on the layer of platinum.

155. (Original) A method according to Claim 153, further comprising the step of forming a layer of a eutectic alloy of AuGe on the layer of gold.

156. (Previously Presented) A method of fabricating a gate structure for a silicon carbide field effect transistor comprising the steps of:

forming an ONO passivation layer on exposed surfaces of a mesa terminated silicon carbide field effect transistor;

forming a gate window in the ONO passivation layer;

forming a gate recess in a channel layer of the mesa terminated silicon carbide transistor; and

forming a gate contact in the gate recess in the channel layer.

157. (Original) A method according to Claim 156, wherein the step of forming an ONO passivation layer comprises the steps of:

high temperature annealing exposed portions of the substrate, p-type epitaxial layer and n-type epitaxial layer in an H_2 ambient; then

forming an SiO_2 layer on the exposed portions of the substrate, p-type epitaxial layer and n-type epitaxial layer; then

argon annealing the SiO_2 layer; then

oxidizing the SiO_2 layer; then

depositing a layer of Si_3N_4 on the oxidized SiO_2 layer; then

oxidizing the layer of Si_3N_4.

158. (Original) A method according to Claim 157, wherein the step of depositing a layer of Si_3N_4 on the oxidized SiO_2 layer is preceded by the step of annealing the oxidized SiO_2 layer in a NO environment.

159. (Original) A method according to Claim 157, wherein the high temperature anneal is carried out at a temperature of greater than about 900 °C for a time of from about 15 minutes to about 2 hours.

160. (Original) A method according to Claim 157, wherein the argon anneal is carried out at a temperature of about 1200 °C for a time of about 1 hour.

161. (Original) A method according to Claim 157, wherein the step of forming an SiO_2 layer comprises the step of forming an SiO_2 layer to a thickness of from about 50 to about 500 Å.

162. (Original) A method according to Claim 157, wherein the step of forming an SiO_2 layer comprises forming an SiO_2 layer through a dry oxide process at a temperature of about 1200 °C.

163. (Original) A method according to Claim 157, wherein the step of oxidizing the SiO_2 layer comprises the step of oxidizing the SiO_2 layer in a wet environment at a temperature of about 950 °C for a time of about 180 minutes.

164. (Original) A method according to Claim 157, wherein the step of depositing a layer of Si_3N_4 comprises the step of depositing a layer of Si_3N_4 to a thickness of from about 200 to about 2000 Å.

165. (Original) A method according to Claim 157, wherein the step of depositing a layer of Si_3N_4 comprises the step of depositing a layer of Si_3N_4 through chemical vapor deposition.

166. (Original) A method according to Claim 157, wherein the step of oxidizing the layer of Si_3N_4 comprises the step of oxidizing the Si_3N_4 layer in a wet environment at a temperature of about 950 °C for a time of about 180 minutes.

167. (Original) A method according to Claim 157, wherein the step of oxidizing the layer of Si_3N_4 comprises the step of oxidizing the Si_3N_4 layer to provide an oxide layer having a thickness of from about 20 to about 200 Å.

168. (Original) A method according to Claim 156, wherein the step of forming a gate contact comprises the step of forming a gate contact in the gate recess utilizing the ONO passivation layer as a mask.

169. (Original) A method according to Claim 168, further comprising the step of patterning the ONO passivation layer so as to provide a ledge in sidewalls of the opening of the ONO passivation layer for the gate recess; and

wherein the step of forming a gate contact in the gate recess comprises the step of forming a mushroom gate structure in the gate recess and on the sidewalls and ledge of the ONO passivation layer.

170. (Original) A method according to Claim 156, wherein the steps of forming a gate window and forming a gate recess are carried out by etching through the ONO passivation layer and into the channel layer by at least one of Electron Cyclotron Resonance and Inductively Coupled Plasma etching.

171. (Original) A method of forming a metal-semiconductor field-effect transistor, comprising:

forming an n-type epitaxial layer of n-type conductivity silicon carbide on a silicon carbide substrate;

forming ohmic contacts on the n-type epitaxial layer that respectively define a source and a drain;

forming a cap layer of n-type silicon carbide on the n-type epitaxial layer;

forming a first recess in the cap layer;

forming a second recess in the n-type epitaxial layer, wherein the recess in the n-type epitaxial layer is within the first recess in the cap layer; and

forming a Schottky metal contact on the n-type epitaxial layer that is between the ohmic contacts and thereby between the source and the drain to form an active channel in the n-type epitaxial layer between the source and the drain when a bias is applied to the Schottky metal contact wherein the Schottky metal contact is within the recess in the n-type epitaxial layer.

172. (Original) A method according to Claim 171, wherein the steps of forming an n-type epitaxial layer and forming a cap layer comprises the step of epitaxially growing the n-type epitaxial layer and the cap layer in a single growth step.

173. (Original) A method according to Claim 172, wherein an n-type dopant concentration in the single growth step is changed to grow the cap layer.

174. (Original) A method according to Claim 171, wherein the step of forming a first recess in the cap layer comprises the step of patterning the cap layer to form the first recess.

175. (Original) A method according to Claim 172, further comprising the steps of:

forming a mesa having sidewalls which extend through the cap layer and the n-type epitaxial layer; and

wherein the step of patterning the cap layer to form the first recess is followed by the steps of:

forming an ONO passivation layer on exposed surfaces of the mesa and the first recess;

forming a gate window in the ONO passivation layer, wherein the gate window is within the first recess;

forming the second recess in n-type epitaxial layer; and

forming a gate contact in the second recess.

176. (Original) A method according to Claim 175, wherein the step of forming an ONO passivation layer comprises the steps of:

high temperature annealing exposed portions of the substrate, p-type epitaxial layer and n-type epitaxial layer in an H_2 ambient; then

forming an SiO_2 layer on the exposed portions of the substrate, p-type epitaxial layer and n-type epitaxial layer; then

argon annealing the SiO_2 layer; then

oxidizing the SiO_2 layer; then

depositing a layer of Si_3N_4 on the oxidized SiO_2 layer; and then

oxidizing the layer of Si_3N_4.

177. (Original) A method according to Claim 176, wherein the step of depositing a layer of Si_3N_4 on the oxidized SiO_2 layer is preceded by the step of annealing the oxidized SiO_2 layer in a NO environment.

178. (Original) A method according to Claim 175, wherein the step of forming a gate contact comprises the step of forming a gate contact in the second recess utilizing the ONO passivation layer as a mask.

179. (Original) A method according to Claim 178, wherein the step of forming a gate contact in the second recess comprises the step of forming a mushroom gate structure in the second recess.

180. (Original) A method according to Claim 175, wherein the steps of forming a gate window and forming a second recess are carried out by etching through the ONO passivation layer and into the n-type epitaxial layer by at least one of Electron Cyclotron Resonance and Inductively Coupled Plasma etching.

181. (Original) A method according to Claim 171, wherein the step of forming a substrate comprises the step of forming a semi-insulating SiC substrate which is substantially free of deep-level dopants.

182. (Original) A method according to Claim 171, further comprising the step of forming a buffer layer between the substrate and the n-type epitaxial layer.

183. (Original) A method according to Claim 182, wherein the step of forming a buffer layer comprises the step of forming an undoped silicon carbide epitaxial layer.

184. (Original) A method according to Claim 182, wherein the step of forming a buffer layer comprises the step of forming an n-type silicon carbide epitaxial layer.

185. (Original) A method according to Claim 182, wherein the step of forming a buffer layer comprises the step of forming a p-type silicon carbide epitaxial layer.

186. (Currently Amended) A method according to Claim [183] 185, wherein the step of forming a p-type epitaxial layer comprises the steps of:

forming a first p-type epitaxial layer on the substrate; and

forming a second p-type epitaxial layer on the first p-type epitaxial layer, wherein the second p-type epitaxial layer has a lower dopant concentration than the first p-type epitaxial layer.

187. (Original) A method according to Claim 185, further comprising the step of forming an ohmic contact to the p-type epitaxial layer.

188. (Original) A method according to Claim 187, further comprising the step of implanting p-type dopants in the p-type epitaxial layer so as to provide a region of p-type conductivity silicon carbide having a higher carrier concentration than the p-type epitaxial layer; and

wherein the step of forming an ohmic contact comprises the step of forming an ohmic contact on the implanted region.

189. (Original) A method according to Claim 187, wherein the step of forming an ohmic contact comprises the steps of:

etching a ground contact window through the cap layer and the n-type epitaxial layer in a region adjacent a source region of the MESFET; and

forming the ohmic contact in the ground contact window.

190. (Original) A method according to Claim 137, wherein the step of depositing a layer of Si_3N_4 comprises the step of depositing a layer of Si_3N_4 to a thickness of from about 200 to about 2000 Å.

191. (Original) A method according to Claim 137, wherein the step of depositing a layer of Si_3N_4 comprises the step of depositing a layer of Si_3N_4 through chemical vapor deposition.